AMENDMENTS TO THE CLAIMS

Claim 1 (Original): A memory cell comprising:

a substrate;

a source region formed in the substrate;

a drain region formed in the substrate;

a channel region provided between the source region and the drain region and having a variable electrical conductivity;

a source-end control gate extending at least partially over a source-end edge section, which adjoins the source region, and being designed to change the electrical conductivity of the source-end edge section;

a drain-end control gate extending at least partially over a drain-end edge section, which adjoins the drain region, and being designed to change the electrical conductivity of the drain-end edge section;

an injection gate arranged between the source-end control gate and the drain-end control gate and extending over a central section of the channel region, the injection gate being electrically isolated from the drain-end control gate and designed to change the electrical conductivity of the central section, which extends between the source-end edge section and the drain-end edge section of the channel region;

a source-end storage element extending at least between the source-end edge section and the source-end control gate;

a drain-end storage element extending at least between the drain-end edge section and the drain-end control gate; and

a gate oxide arrangement having at least one gate oxide layer extending between the substrate on the one side and the source-end control gate, the drain-end control gate and the injection gate on the other side, wherein the source-end control gate and the drain-end control gate are electrically connected to one another.

Claim 2 (Original): The memory cell according to Claim 1, wherein the storage element includes silicon nitride.

Claim 3 (Original): The memory cell according to Claim 1, wherein the storage element includes silicon dioxide.

Claim 4 (Original): The memory cell according to Claim 1, wherein at least one of the source-end storage element and the drain-end storage element is an integrated part of an ONO layer, which is formed from a first silicon dioxide layer, a silicon nitride layer formed on the first silicon dioxide layer, and a second silicon dioxide layer formed on the silicon nitride layer.

Claim 5 (Original): The memory cell according to Claim 4, wherein the gate oxide layer is formed of single-piece construction with the first silicon dioxide layer.

Claim 6 (Original): The memory cell according to Claim 1, wherein the channel region has an n-type channel.

Claim 7 (Original): The memory cell according to Claim 1, wherein the channel region has a p-type channel.

Claim 8 (Original): A method for programming a memory cell as defined in Claim 1, wherein an electrical source voltage with a source voltage value is applied to the source region, and an electrical drain voltage with a drain voltage value is applied to the drain region, the source voltage value and the drain voltage value being different, comprising the steps of:

applying an electrical injection gate voltage with an injection gate voltage value to the injection gate;

applying an electrical source-control-gate voltage with a source-control-gate voltage value to the source-end control gate; and

applying an electrical drain-control-gate voltage with a drain-control-gate voltage value to the drain-end control gate;

wherein the drain-control-gate voltage value and the source-control-gate-voltage value are the same and the source-control-gate voltage value and the drain-control-gate voltage value each have a greater absolute value than the injection gate voltage value.

Claim 9 (Original): A method for erasing a memory cell as defined in Claim 1, wherein an electrical source voltage with a source voltage value is applied to the source region, and an electrical

drain voltage with a drain voltage value is applied to the drain region, the source voltage value and the drain voltage value being different, comprising the steps of:

applying an electrical injection gate voltage with an injection gate voltage value to the injection gate;

applying an electrical source-control-gate voltage with a source-control-gate voltage value to the source-end control gate; and

applying an electrical drain-control-gate voltage with a drain-control-gate voltage value to the drain-end control gate;

wherein the drain-control-gate voltage value and the source-control-gate-voltage value are the same and the source-control-gate voltage value and the drain-control-gate voltage value each have a greater absolute value than the injection gate voltage value.

Claim 10 (Original): A method for programming a memory cell as defined in Claim 1, comprising the steps of:

applying a first electrical voltage to the injection gate; and

applying a second electrical voltage to each of the source-end control gate and the drain-end control gate,

wherein the second electrical voltage has a greater absolute value that the first electrical voltage.

Claim 11 (Canceled)